A Low-power Low-cost Optical Router for Optical Networks-on-Chip in Multiprocessor Systems-on-Chip

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***Abstract*---Networks-on-chip (NoCs) can improve the communication bandwidth and power efficiency of multiprocessor systems-on-chip (MPSoC). However, traditional metallic interconnects consume significant amount of power to deliver even higher communication bandwidth required in the near future. Optical NoCs are based on optical interconnects and optical routers, and have significant bandwidth and power advantages. This paper proposed a high-performance low-power low-cost optical router, Cygnus, for optical NoCs. Cygnus is non-blocking and based on silicon microresonators. We compared Cygnus with other microresonator-based routers, and analyzed their power consumption, optical power insertion loss, and the number of microresonators used in detail. The results show that Cygnus has the lowest power consumption and losses, and requires the lowest number of microresonators. For example, Cygnus has 50% less power consumption, 51% less optical power insertion loss, and 20% less microresonators than the optimized traditional optical crossbar router. Comparing to a high-performance 45nm electronic router, Cygnus consumes 96% less power. Moreover, the passive routing feature of Cygnus guarantees that, while using dimension order routing algorithm, the maximum power consumption to route a packet through a network is a small constant number, regardless of the network size. For example, the maximum power consumption is 4.80fJ/bit under current technologies. We simulated and analyzed an 8x8 2D mesh NoC built from Cygnus and showed the end-to-end delay and network throughput under different offered loads and packet sizes.**

I. INTRODUCTION

On-chip communications are facing new challenges in the gigascale multiprocessor system-on-chip (MPSoC) paradigm [1]. As the complexity of MPSoC increases, on-chip communication cost also increases [2]. Moreover, while shrinking feature sizes reduce gate delays exponentially over each technology generation, global metallic wire delays increase exponentially at the same time. Traditional on-chip communication techniques for SoCs face several issues, such as poor scalability, limited bandwidth, and low utilization [3]. Networks–on-chip (NoCs) use modern communication and networking theories to relieve these issues [4][5][6][7].

New technologies, such as nanotechnologies, continually reduce the feature sizes, while new SoC applications demand even more on-chip communications. The conventional metallic interconnect gradually becomes the bottleneck of NoC performance due to the limited bandwidth, long delay, large area, and high power consumption. Optical interconnect networks have demonstrated their strength in multicomputer systems, on-board inter-chip interconnect, switching fabrics in core routers, and etc. Optical NoCs are based on on-chip optical interconnects and routers [8]. They are promising candidates to overcome the limitations of traditional metallic-interconnect-based NoCs [9].

Optical router is the heart of an optical NoC. The progress in photonic technologies, especially the development of microresonators, makes optical on-chip routers possible [19]. Microresonators can be fabricated on silicon-on-insulator (SOI) substrates, which have been used for CMOS-based high-performance low-leakage SoCs. They are as small as 3μm in diameter [11]. Microresonators are a good candidate for very large scale integrated optoelectronic circuits, and can be used as optical switch, optical add-drop multiplexer (OADM), modulator, and optical sensor.

Optical routers implement the routing and flow control functions, and switch packets from an input port to an output port using an optical switching fabric. The optical switching fabric is usually composed of multiple basic optical switching elements, which implement the basic 1x2, 2x1, or 2x2 switching functions. A control unit commands the optical switching fabric based on routing requests and a routing algorithm. The control unit can be built from CMOS transistors to process routing requests. For microresonator-based routers, the control unit uses electrical signals to control basic optical switching elements.

Several optical on-chip routers are designed based on microresonators. M. Briere et al. proposed the λ-router [12]. λ-router uses a passive switching fabric and wavelength-division multiplexing (WDM) technology. An NxN λ-router needs N wavelengths and multiple basic 2x2 switching elements to realize non-blocking switching function. The λ-router prefers N to be an even number to fully utilize all the components. A. Shacham et al. proposed an optical NoC architecture, called photonic NoC, including the topology, routing and flow control algorithm, and building blocks [9]. The photonic NoC is built from 4x4 routers, injection switches, and ejection switches. The injection and ejection switches are used for local injection and ejection packets. We proposed an optimized 4x4 optical router for fat tree-based optical NoC [10]. A. W. Poon et al. proposed a non-blocking 5x5 optical router based on an optimized crossbar [13]. Each port of the router is aligned to its corresponding direction to reduce the waveguide crossings around the switching fabric.

In this paper, we propose a novel non-blocking 5x5 optical router, Cygnus, for optical NoCs. Compared with other routers, Cygnus uses the lowest number of microresonators, consumes the least power, and has the lowest optical power insertion loss. Cygnus improves the scalability of optical NoCs by passively

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routing packets which travel in one dimension and only actively routing packets which make turns. Particularly, while using the dimension order routing, this design guarantees that the maximum power consumption to route packets through a network is a small constant number, regardless of the network size. The following section presents the design details of Cygnus. The characteristics of Cygnus are analyzed and compared with other optical routers in Section 3. Section 4 shows the simulation results and analyzes the performance of an 8x8 2D mesh optical NoC using Cygnus. Section 5 concludes the paper.

II. CYGNUS ROUTER

Cygnus is based on two types of basic switching elements which use microresonators. We will briefly introduce the working princeples of the microresonators and switching elements before detailing the router.

A. Microresonator and Basic 1x2 Switching Elements

Two types of basic 1x2 switching elements are used including the parallel switching element and crossing switching element (Fig. 1). They both consist of two waveguides and one microresonator. When the microresonators are powered on and off, the corresponding optical paths are highlighted in Figure 1. When powered off, a microresonator has an off-state resonance wavelength λ_{off}, which is determined by the material and structure of the microresonator. When the microresonator is powered on, the resonance wavelength changes to the on-state resonance wavelength λ_{on}. While the microresonator is powered off, an incident light signal with wavelength λ_{on} will propagate from the input port to the through port. On the other hand, while the microresonator is powered on, the incident light from the input port will be coupled into the microresonator and directed to the drop port. This mechanism implements a 1x2 switching function. When using a single wavelength λ_{on}, the add port serves as an additional input port, which is restricted to be used only if the other input port is not used or the microresonator is powered off.

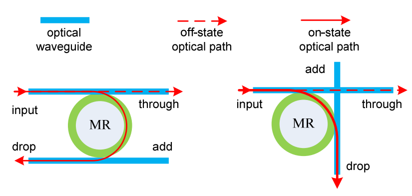

Fig.1. Basic 1x2 switching elements using microresonators: (a) parallel switching element, (b) crossing switching element

The main difference of the two basic 1x2 switch elements is the positions of the waveguides. Compared with the crossing switching element, the parallel switching element does not have any waveguide crossing. Optical waveguide crossings introduce non-negligible crossing insertion loss. The waveguide crossing insertion loss is 0.12dB per crossing [13]. Although, the crossing insertion loss is relative small, there are a large number of crossings in an optical NoC. In the on state, the microresonator needs a DC current, and its power consumption is less than 20μW [13]. In the off-state, no power will be consumed by the microresonator, if ignoring the small bias voltages to mitigate process variations. The power consumption of the microresonator is expected to decrease with continual improvement of its material and structure. The switching time of the microresonator is small, and a 30ps switching time has been demonstrated [14].

B. Cygnus Router Architecture

Cygnus is a strictly non-blocking optical 5x5 router for optical NoC (Fig. 2). It consists of a switching fabric and a control unit which uses electrical signals to configure the switching fabric according to the routing requirement of each packet. The switching fabric is built from the two basic switching elements. Cygnus uses only 16 microresonators, six waveguides, and two waveguide terminators. The microresonators in the switching fabric are identical, and have the same on-state and off-state resonance wavelengths, λ_{on} and λ_{off}. Cygnus uses a single wavelength which corresponds to λ_{on}. An additional microresonator can be reduced by replacing the last microresonator on the waveguide for the injection port with a Y-branch. Although this reduced the number of microresonators and save power, more loss will be encountered by packets which exist from the east port. The non-blocking property of Cygnus is proved by enumerating all possible cases.

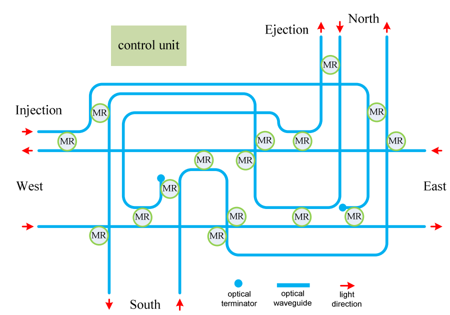

Fig. 2. Cygnus router

Cygnus has five bidirectional ports, including injection/ejection, west, south, east, and north. The injection/ejection port connects a functional core through an optical/electronic (O/E) interface. The functional core could be a processor, MPEG decoder, memory controller, etc. The five ports are aligned to their intended directions, and the input and output of each port is also properly aligned to ensure that no extra crossing are required while one Cygnus router connect to another in 2D optical NoCs in most cases. The switching fabric implements a 5x5 switching function for the five bidirectional ports. U-turn function is not implemented because routing and flow control algorithms normally avoid it. The internal structure of the switching fabric is designed to minimize waveguide crossings. Different from other optical routers, Cygnus takes the advantage of the parallel switch element to minimize insertion loss. Especially, the two waveguides for the injection/ejection port only use the parallel switching elements.

Cygnus is designed to passively route packets which travel in one dimension. Packets, traveling between south and north as well as east and west, do not require to power on any microresonator. And only one microresonator is powered on when a packet uses the injection/ejection port or makes a turn. This feature is beneficial to large networks and network scalability. It not only reduces the power consumption but also avoids the high microresonator insertion loss for routing algorithms which limit the number of turns. In particular, while using the dimension order routing, this feature guarantees that the maximum power consumption to route packets through a network is a small constant number, regardless of the network size. This is because that networks built from Cygnus only need to power on at most three microresonators to inject, turn, and eject a packet in dimension order routing. As we will see in the following section, the constant number is very small and close to the average power consumption.

The switching fabric is configured by the control unit. The control unit is built from traditional CMOS transistors and uses electrical signals to power on and off each microresonator according to the routing requirement of each packet based on routing and flow control algorithm. The control units of all the Cygnus routers in an optical NoC use an electronic network to setup and maintain optical paths.

III. Analysis and Comparisons

We analyzed and compared Cygnus with other optical routers including the λ-router, optimized crossbar router, traditional crossbar router, and router proposed in [9], which is referred to as CR for clarity. We analyzed the important characteristics of the above optical routers, including the power consumptions, optical power insertion losses, and the required numbers of microresonators.

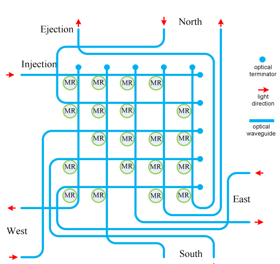

Fig.3 Traditional 5x5 crossbar with aligned ports and without U-turns

The switching fabric of an optical router can be implemented using the traditional full-connected crossbar. An NxN optical router, which does not support U-turns, requires an NxN crossbar, which is composed of N(N-1) microresonators, 2N crossing waveguides, and 2N optical terminators (Fig. 3). To use the traditional crossbar in a regular topology NoC, ports have to align to corresponding directions. We assigned the ports for the traditional crossbar to avoid internal waveguide crossings while minimizing the waveguide crossings during port alignment. The traditional full-connected crossbar can be further optimized by reorienting the internal structure for port alignment. The optimized crossbar reduces waveguide crossings, but does not improve the power efficiency over the traditional crossbar. Since NoCs with regular 2D topologies require 5x5 routers and the λ-router only supports even numbers of input and output ports, a 6x6 λ-router is used in the comparison with one pair of idle input and output ports.

A. *Number of Microresonators*

The number of microresonators used by an optical router decides its area cost along with its floorplan. Lowering the number of microresonators will reduce die size and increase yield, which, in turn, will lower chip cost. We compared the numbers of microresonator required to implement the five optical routers. Cygnus uses the lowest number of microresonators, 16, which is 20% less than the traditional crossbar (Fig. 4). Since λ-router uses a multistage switching fabric and two ports are unused, it requires the largest number of microresonators.

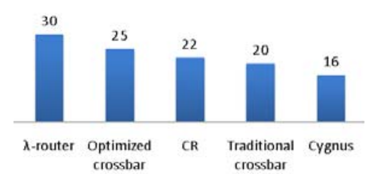

Fig. 4. The number of microresonators

B. *Power Consumption*

Power consumption is a critical aspect of optical on-chip router design. For high-performance computing, low power consumption can reduce the cost related with packing, cooling solution, testing, and system integration. We concentrate on switching fabric in this section, and assume that the control units of the routers implemented the same routing algorithm and hence consume the same power. Since the λ-router uses WDM and a passive switching fabric, it requires extra units for wavelength selection or conversion, which the authors did not reveal the design details. Due to incomplete information, we could not compare the power consumption of λ-router with other routers.

We can analyze an optical router from two different angles. The first angle is analyzing a stand-alone router. Due to the asymmetrical architecture of an optical router, a packet taking different input and output ports will require different amount of power to route it. All the five optical routers require to power on at most one microresonator to route a packet. The second angle is to analyze a router as a part of a network and study the impacts of different router architectures at network level. We analyzed the power efficiency of the five optical routers in a 8x8 2D mesh NoC using dimension order routing. The power efficiency is measured in two ways, the average power consumption per optical path and the average power consumption per router. The average power consumption per optical path E_p is calculated using the equation (1). M is the total number of optical paths in a network. E_i is the power consumed on the i-th path when the bandwidth is B. The average power consumption per router E_r is calculated by dividing E_p by the average number of routers on all the optical paths. We assume a moderate bandwidth of 12.5Gbit/s for each optical path in the network.

$$E_p = \frac{\sum_{i=1}^{M} E_i}{M \times B} \tag{1}$$

Network-level analysis shows that Cygnus has the lowest average power consumption per path, 4.80fJ/bit, which is 50% less than the two crossbar architectures (Fig. 5). On average, a Cygnus router only consumes 0.76fJ/bit. A further analysis shows that the maximum power consumption of Cygnus in the network is also 4.80fJ/bit. This coincidence is due to most packets in a network based on Cygnus needs the same amount of power to route and the limited precision of the two numbers hides the small difference.

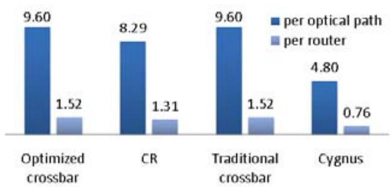

Fig. 5. Average power consumption on a path and a router (fJ/bit)

Regardless the size of a network, Cygnus has a constant maximum power consumption while using dimension order routing. This can be proved as follows. According to the architecture, Cygnus does not need to power on any microresonator for a packet traveling along a column or row. Cygnus only powers on one microresonator when a packet enters a network from an injection port, turns from a row to a column, or exits the network from an ejection port. In the worst case, at most three microresonators are powered on to route a packet in a network based on Cygnus, and this number does not change with the network size. This feature allows an optical network based on Cygnus scales without worrying the power consumed by the additional routers on a longer path. In comparison, a network based on the other routers does not scale well.

C. *Insertion Loss*

Insertion losses of an optical router decide its feasibility as well as the power consumption required by the O/E interfaces to generate, modulate, and detect optical signals. In our comparison, we considered two major sources of optical insertion losses, the waveguide crossing insertion loss and microresonator insertion loss. The microresonator insertion loss is 0.5dB [15]. We consider the waveguide crossings both inside and outside switching fabrics. Similar to the power analysis, we studied the insertion loss of a router from two angles, analyzing a stand-alone router and a router as a part of a network. The waveguide propagation loss is only 0.17dB/mm [16], and we omit it because all the routers are compared in the same NoC and silicon die sizes are usually in the order of 10mmx10mm.

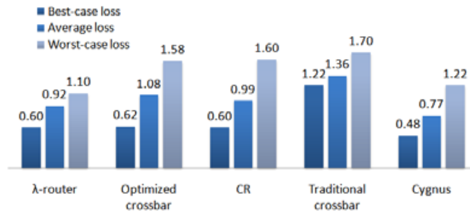

Fig. 6. The best-case, worst-case, and average losses (dB)

Different input-output pairs of an optical router may have different losses. We compared the worst-case loss, best-case loss, and average loss of all possible cases (Fig. 6). The result shows that Cygnus has the lowest losses in all the categories. Cygnus has 61% less best-case loss, 43% less average loss, and 28% less worst-case loss than the traditional crossbar. We also compared the average loss of the longest paths in the 8x8 2D mesh NoC based on dimension order routing (Fig. 7). Cygnus still has the lowest loss in this comparison, while the traditional crossbar has the highest loss. Cygnus has 51.7% less average longest path loss than the full-connected crossbar. If we mark the routers in the four corners as router (0, 0), (0, 7), (7, 0), and (7, 7) respectively in the 8x8 2D mesh NoC, the longest paths for XY routing algorithm are between router (0, 0) and (7, 7) and router (0, 7) and (7, 0). We analyzed the longest path loss for the five routers similarly. For Cygnus, a packet is sent from

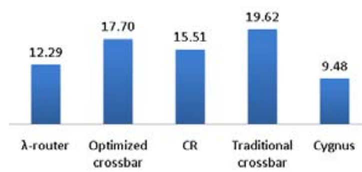

Fig. 7. Average longest path loss (dB)

router (0, 7) to (7, 0). The packet enters NoC from the injection port to the east port, and encounters four waveguide crossings and one resonator. So the loss is 0.12x4+0.5=0.98dB. In the second router (1, 7) on the path, four waveguide crossings are encountered, so the loss is 0.12x4=0.48dB. This is the same case for the following five routers (2, 7), (3, 7)…… (6, 7). In the corner router (7, 7), one resonator is encountered, so the loss is 0.5dB. Similarly, there are six crossings in router (7, 6), (7, 5), …, and (7, 1) each, so the loss is 0.12x6=0.72dB. At the destination router (7, 0), one resonator is encountered, so the loss is 0.5dB. Therefore, the total loss in the longest path is to 9.18dB. After calculating the losses for all the longest paths, the average longest path is 9.48dB.

D. *Electronic vs. Optical Router*

We designed and simulated a 5x5 input-buffered pipelined electronic router (Fig. 8). The design is based on the 45nm Nangate open cell library and Predictive Technology Model [17]. Each port of the electronic router is 32-bit wide. The router implements the dimension order routing algorithm. The switching fabric is a crossbar. We model the metal wires in the crossbar as a fine-grained lumped RLC network, and consider the coupling capacitance. Since the coupling inductance has a significant effect at deep submicron process technologies, mutual inductances are considered up to the third neighboring wire.

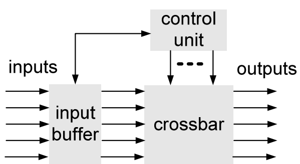

Fig. 8. 5x5 input-buffered pipelined electrical router

To compare with the optical routers, we designed the electrical router to deliver the same maximum throughput as the optical router. We choose a moderate 12.5Gbit/s for each port. The electronic router is simulated in Cadence Spectre. The simulation results show that on average the crossbar consumes 0.07pJ/bit, the input buffer consumes 0.003pJ/bit, and the control unit consumes 1pJ to make decisions for each packet. The optical routers implement the same routing algorithm, and do not have input buffers. Without considering the input buffer, all the studied optical routers consume one to two orders of magnitude lower power than the electronic router. In particular, Cygnus only consumes 3.8% power of the high-performance electronic router, while routing 512-bit packets.

IV. Simulation Results

We built an 8x8 2D mesh optical NoC using Cygnus, and studied its performance (Fig. 9). Since static optical memory is difficult to build, to avoid costly optical-electronic conversions while using electronic memories, the optical NoC only use electronic memories as buffers at the network interfaces between functional cores and the optical NoC. We separate the control information from payload and put them in control packets and payload packets respectively. Payload packets carry data and processor instructions, while control packets carry the network control information. The optical NoC consists of two overlapped networks, an optical network for payload packets and an electronic network for control packets. The electronic network connects the control units of all the Cygnus routers in the same topology as the optical network. In general, the topologies of the two networks can be different. While payload packets use circuit switching in the optical network, control packets use packet switching in the electronic network to setup and maintain the circuit switching paths.

The optical NoC uses dimension order routing for a control packet, which setups an optical path along the course for the corresponding payload packet. When the control packet reach its destination, an acknowledge packet is sent backward to the source and activates optical routers on the path. Once receiving the acknowledge packet, the source sends the payload packet. The source sends a termination packet along with the last flit of the payload packet, which releases the optical path. In dimension order routing, each packet is routed first in X dimension until it reach the node, which is in the same column with the destination, and then along the perpendicular Y dimension to the destination. Dimension order routing is a minimal path routing algorithm. In addition, it is a low-complexity distributed algorithm without using any routing table. These features make dimension order routing particularly suitable for NoCs, which require low latency and low cost at the same time. It has been used by many practical systems, and favored by many NoC studies.

The optical and metallic interconnects are all bidirectional. While the optical interconnects are 1-bit wide on each direction, metallic interconnects are 32-bit wide on each direction. In the optical NoC, processors generate packets independently and at time intervals following a negative exponential distribution. We used the uniform traffic pattern, i.e. each processor sends packets to all other processors with the same probability. The optical NoC is simulated using a network simulator, OPNET [18]. We assumed a moderate peak bandwidth, 12.5Gbit/s, for each injection port. 12.5Gbit/s can be achieved by using a single modulator based on microresonators [14].

The performance of the optical NoC is measured in terms of end-to-end (ETE) delay and throughput. The ETE delay is the average time between processors generating packets and the packets reaching destinations. It is the sum of the connection-oriented path-setup time and the time used to transmit optical packets. The throughput of the optical NoC measures the total

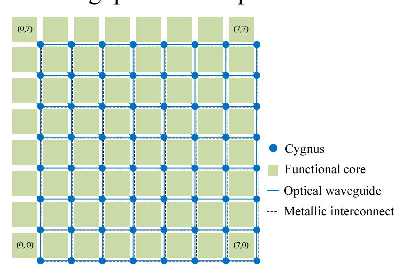

Fig. 9. 8x8 2D mesh optical NoC based on Cygnus

throughput of the network under a given offered load. Following the definition, offered load α can be calculated as in equation (2). $T_{transmission}$ is the time that a network spend to transmit packets, and T_{gap} is an exponentially distributed time between two packets. We simulated a range of packet sizes used by typical SoC applications, and use the size of 32-bit for path-setup and acknowledge packets.

$$\alpha = \frac{T_{transmission}}{T_{transmission} + T_{gap}} \quad (2)$$

The ETE delay under different offered load is shown in Fig. 10. The network saturates at different loads with different packet sizes. The ETE delay is very low before the saturation load, and increases dramatically after it. For the 512B packets, ETE delay is 30ns before the saturation load 0.18, and goes up quickly after the saturation load. Packets larger than 8B have much higher saturation load. In dimension order routing, each payload packet corresponds to two control packets, one path-setup packet and one acknowledge packet. Under the same offered load, larger packets cause the network to use less control packets compared with smaller packets. Larger packets also have longer transmission times and cause longer inter-packet arrival gaps compared with smaller packets under the same offered load. Long inter-packet arrival gaps can reduce network blocking during path setup. The combined effect makes larger packets suffer from less congestion, and hence have higher saturation loads than smaller packets. As the packet size increases, the difference between the ETE delay curves of adjacent packet sizes becomes smaller. Little delay improvement can be achieved for the packet sizes larger than 512B, because a balance point has been reached between the

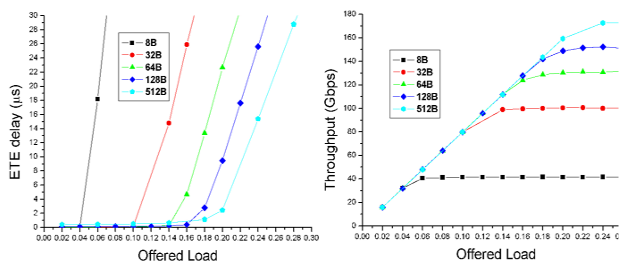

Fig. 10. ETE delay and throughput

effect of longer transmission time and the influence of contention in path-setup procedures. The balance point is decided by the mesh topology, dimension order routing algorithm, and traffic pattern. Fig. 10 also shows the network throughput under different offered load using the different packet sizes. The trend concluded from ETE delay can be obtained more clearly here.

V. Conclusion

This paper proposed a low-power, low-loss, and low-cost 5x5 optical router, Cygnus, for optical NoCs. Cygnus is non-blocking and based on silicon microresonators. Cygnus is compared with other optical routers. The comparison results show that Cygnus has the lowest power consumption and losses and requires the lowest number of microresonators. For example, Cygnus consumes 50% less power, has 51% less loss, and requires 20% less microresonators than the traditional crossbar. Cygnus consumes only 3.8% power of the high-performance 45nm electronic router. While using dimension order routing, Cygnus can guarantee the maximum power to route a packet through a network to be a small constant number, regardless of the network size. The number is 4.80fJ/bit under current technology. Furthermore, the maximum power consumption is very close to the average power consumption. We simulated an 8x8 2D mesh NoC based on Cygnus and dimension order routing, and showed the ETE delay and network throughput under different traffic loads and packet sizes, which are typically used in SoC applications.

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References

[1] L. Benini, G. De Micheli, “Networks on chip: A new paradigm for systems on chip design”, *Design, Automation and Test in Europe Conference and Exhibition*, 2002.

[2] S. Li, L. Peh, A. Kumar, and N. K. Jha, "Temperature-Aware On-Chip Networks," *IEEE Micro*, vol. 26, pp. 130-139, 2006.

[3] J. Henkel, W. Wolf, S. T. Chakradhar, “On-chip networks: A scalable, communication-centric embedded system design paradigm”, *in Proc. 17th International Conference on VLSI Design*, 2004.

[4] S. Kumar, A. Jantsch, J.P. Soininen, M. Forsell, M. Millberg, J. Öberg, K. Tiensyrjä, and A. Hemani, “A network on chip architecture and design methodology”, *IEEE Computer Society Annual Symposium on VLSI*, 2002.

[5] J. Xu, W. Wolf, J. Henkel, and S. Chakradhar, “A Design Methodology for Application-Specific Networks-on-Chip”, *ACM Transactions on Embedded Computing Systems*, July 2006.

[6] K. Goossens, J. Dielissen, A. Radulescu, “Æthereal network on chip: Concepts, architectures and implementations”, *IEEE Design Test Comput*, Vol.22, No.5, pp414–421. 2005.

[7] K. Srinivasan, K. S. Chatha, and G. Konjevod, "Application Specific Network-on-Chip Design with Guaranteed Quality Approximation Algorithms," *Asia and South Pacific Design Automation Conference*, pp. 184-190, 2007.

[8] M. Haurylau, G. Chen, H. Chen, J. Zhang, N.A. Nelson, D.H. Albonesi, E.G. Friedman, P.M. Fauchet, "On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions," *IEEE Journal of Selected Topics in Quantum Electronics,* vol.12, no.6, pp.1699-1705, 2006.

[9] A. Shacham, B.G. Lee, A. Biberman, K. Bergman, L.P. Carloni, “Photonic NoC for DMA Communications in Chip Multiprocessors”, *Hot Interconnects*, 2007.

[10] H. Gu, W. Zhang, J. Xu, “A Low-power Fat Tree-based Optical Network-on-Chip for Multiprocessor System-on-Chip”, *Design, Automation and Test in Europe Conference and Exhibition*, 2009.

[11] B. E. Little, J. S. Foresi, G. Steinmeyer *et al.*, “Ultra-compact Si-SiO_2 microring resonator optical channel dropping filters,” *IEEE Photonics Technology Letters,* vol. 10, no. 4, pp. 549-551, 1998.

[12] M. Briere, B. Girodias, et al, “System Level Assessment of an Optical NoC in an MPSoC Platform”, *Design, Automation & Test in Europe Conference & Exhibition*, 2007.

[13] A. W. Poon, F. Xu, X. Luo, “Cascaded active silicon microresonator array cross-connect circuits for WDM networks-on-chip”, in Proc. SPIE Int. Soc. Opt. Eng. 6898, 689812, 2008.

[14] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, M. Lipson, “12.5 Gbit/s carrier injection-based silicon microring silicon modulators”, *Optics Express*, Vol.15, No.2, pp430–436, 2007.

[15] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for WDM applications," *Optics Express*, vol. 15, pp. 7489-7498, 2007.

[16] F. Xia, L. Sekaric, and Y. Vlasov, “Ultracompact optical buffers on a silicon chip,” *Nature Photonics*, 65-71, 2007.

[17] https://www.si2.org/openeda.si2.org/projects/nangatelib/

[18] www.opnet.com

[19] Q. Xu, B. Schmidt, S. Pradhan, M. Lipson, “Micrometre-scale silicon electro-optic modulator”, *Nature*, Vol.435, No.7040, pp325-327, 2005.